THAT WHICH IS CLAIMED IS:

1. A method for making a semiconductor device comprising:

forming a superlattice comprising a plurality of stacked groups of layers; and

forming regions for causing transport of charge carriers through the superlattice in a parallel direction relative to the stacked groups of layers;

each group of layers of the superlattice comprising a plurality of stacked base semiconductor monolayers defining a base semiconductor portion and an energy band-modifying layer thereon;

the energy-band modifying layer comprising at least one non-semiconductor monolayer constrained within a crystal lattice of adjacent base semiconductor portions so that the superlattice has a higher charge carrier mobility in the parallel direction than would otherwise be present.

2. A method according to Claim 1 wherein the superlattice also has a common energy band structure therein.

3. A method according to Claim 1 wherein the charge carriers having the higher mobility comprise at least one of electrons and holes.

4. A method according to Claim 1 wherein each base semiconductor portion comprises silicon.

5. A method according to Claim 1 wherein each energy band-modifying layer comprises oxygen.

6. A method according to Claim 1 wherein each energy band-modifying layer is a single monolayer thick.

7. A method according to Claim 1 wherein each base semiconductor portion is less than eight monolayers thick.

8. A method according to Claim 1 wherein each base semiconductor portion is two to six monolayers thick.

9. A method according to Claim 1 wherein the superlattice further has a substantially direct energy bandgap.

10. A method according to Claim 1 wherein the superlattice further comprises a base semiconductor cap layer on an uppermost group of layers.

11. A method according to Claim 1 wherein all of the base semiconductor portions are a same number of monolayers thick.

12. A method according to Claim 1 wherein at least some of the base semiconductor portions are a different number of monolayers thick.

13. A method according to Claim 1 wherein all of the base semiconductor portions are a different number of monolayers thick.

14. A method according to Claim 1 wherein each non-semiconductor monolayer is thermally stable through deposition of a next layer.

15. A method according to Claim 1 wherein each base semiconductor portion comprises a base semiconductor selected from the group consisting of Group IV semiconductors, Group III-V semiconductors, and Group II-VI semiconductors.

16. A method according to Claim 1 wherein each energy band-modifying layer comprises a non-semiconductor selected from the group consisting of oxygen, nitrogen, fluorine, and carbon-oxygen.

17. A method according to Claim 1 wherein forming the superlattice comprises forming the superlattice on a substrate.

18. A method according to Claim 1 wherein the higher charge carrier mobility results from a lower conductivity effective mass for charge carriers in the parallel direction than would otherwise be present.

19. A method according to Claim 18 wherein the lower conductivity effective mass is less than two-thirds the conductivity effective mass that would otherwise occur.

20. A method according to Claim 1 further comprising doping the superlattice with at least one type of conductivity dopant therein.

21. A method according to Claim 1 wherein the superlattice defines a channel for the semiconductor device and wherein forming the regions comprises:

forming source and drain regions laterally adjacent the superlattice channel; and

forming a gate overlying the superlattice channel.

22. A method for making a semiconductor device comprising:

forming a superlattice comprising a plurality of stacked groups of layers; and

forming regions for causing transport of charge carriers through the superlattice in a parallel direction relative to the stacked groups of layers;

each group of layers of the superlattice comprising a plurality of stacked silicon atomic layers defining a silicon portion and an energy band-modifying layer thereon;

the energy-band modifying layer comprising at least one oxygen atomic layer constrained within a crystal lattice of adjacent silicon portions so that the superlattice has a higher charge carrier mobility in the parallel direction than would otherwise be present.

23. A method according to Claim 22 wherein the superlattice has a common energy band structure therein.

24. A method according to Claim 22 wherein the charge carriers having the higher mobility comprise at least one of electrons and holes.

25. A method according to Claim 22 wherein each energy band-modifying layer is a single atomic layer thick.

26. A method according to Claim 22 wherein each silicon portion is less than eight atomic layers thick.

27. A method according to Claim 22 wherein each silicon portion is two to six atomic layers thick.

28. A method according to Claim 22 wherein the superlattice further has a substantially direct energy bandgap.

29. A method according to Claim 22 wherein the superlattice further comprises a silicon cap layer on an uppermost group of layers.

30. A method according to Claim 22 wherein all of the silicon portions are a same number of atomic layers thick.

31. A method according to Claim 22 wherein at least some of the silicon portions are a different number of atomic layers thick.

32. A method according to Claim 22 wherein all of the silicon portions are a different number of atomic layers thick.

33. A method according to Claim 22 wherein forming the superlattice comprises forming the superlattice on a substrate.

34. A method according to Claim 22 wherein the higher charge carrier mobility results from a lower conductivity effective mass for charge carriers in the parallel direction than would otherwise be present.

35. A method according to Claim 22 further comprising doping the superlattice with at least one type of conductivity dopant therein.

36. A method according to Claim 22 wherein the superlattice defines a channel for the semiconductor device and wherein forming the regions comprises:

forming source and drain regions laterally adjacent the superlattice channel; and

forming a gate overlying the superlattice channel.

37. A method for making a semiconductor device comprising:

forming a superlattice comprising a plurality of stacked groups of layers; and

forming regions adjacent the superlattice for causing transport of charge carriers through the superlattice in a parallel direction relative to the stacked groups of layers;

each group of layers of the superlattice comprising less than eight stacked base semiconductor

monolayers defining a base semiconductor portion and an energy band-modifying layer thereon;

the energy-band modifying layer comprising a single non-semiconductor monolayer constrained within a crystal lattice of adjacent base semiconductor portions so that the superlattice has a higher charge carrier mobility in the parallel direction than would otherwise be present.

38. A method according to Claim 37 wherein the superlattice has a common energy band structure therein.

39. A method according to Claim 37 wherein the charge carriers having the higher mobility comprise at least one of electrons and holes.

40. A method according to Claim 37 wherein the superlattice further has a substantially direct energy bandgap.

41. A method according to Claim 37 wherein the superlattice further comprises a base semiconductor cap layer on an uppermost group of layers.

42. A method according to Claim 37 wherein all of the base semiconductor portions are a same number of monolayers thick.

43. A method according to Claim 37 wherein at least some of the base semiconductor portions are a different number of monolayers thick.

44. A method according to Claim 37 wherein all of the base semiconductor portions are a different number of monolayers thick.

45. A method according to Claim 37 wherein forming the superlattice comprises forming the superlattice on a substrate.

46. A method according to Claim 37 wherein the higher charge carrier mobility results from a lower conductivity effective mass for charge carriers in the parallel direction than would otherwise be present.

47. A method according to Claim 37 further comprising doping the superlattice with at least one type of conductivity dopant therein.

48. A method according to Claim 37 wherein the superlattice defines a channel for the semiconductor device and wherein forming the regions comprises:

forming source and drain regions laterally adjacent the superlattice channel; and

forming a gate overlying the superlattice channel.

49. A method for making a semiconductor device comprising:

forming a superlattice comprising a plurality of stacked groups of layers; and

forming regions for causing transport of charge carriers through the superlattice in a parallel direction relative to the stacked groups of layers;

each group of layers of the superlattice comprising less than eight stacked silicon atomic layers defining a silicon portion and an energy band-modifying layer thereon;

the energy-band modifying layer comprising a single oxygen atomic layer constrained within a crystal lattice of adjacent silicon portions.

50. A method according to Claim 49 wherein the superlattice further comprises a base semiconductor cap layer on an uppermost group of layers.

51. A method according to Claim 49 wherein all of the base semiconductor portions are a same number of atomic layers thick.

52. A method according to Claim 49 wherein at least some of the base semiconductor portions are a different number of atomic layers thick.

53. A method according to Claim 49 wherein all of the base semiconductor portions are a different number of monolayers thick.

54. A method according to Claim 49 wherein forming the superlattice comprises forming the superlattice on a substrate.

55. A method according to Claim 49 further comprising doping the superlattice with at least one type of conductivity dopant therein.

56. A method according to Claim 49 wherein the superlattice defines a channel for the semiconductor device and wherein forming the regions comprises:

forming source and drain regions laterally adjacent the superlattice channel; and

forming a gate overlying the superlattice channel.

57. A method for making a semiconductor device comprising:

forming a superlattice comprising a plurality of stacked groups of layers; and

forming regions for causing transport of charge carriers through the superlattice in a parallel direction relative to the stacked groups of layers;

each group of layers of the superlattice comprising a plurality of stacked base semiconductor monolayers defining a base semiconductor portion and an energy band-modifying layer thereon;

the energy-band modifying layer comprising at least one non-semiconductor monolayer constrained within a crystal lattice of adjacent base semiconductor portions so that the superlattice has a lower conductivity effective mass for charge carriers in the parallel direction than would otherwise be present.

58. A method according to Claim 57 wherein the superlattice also has a common energy band structure therein.

59. A method according to Claim 57 wherein the charge carriers having the lower conductivity effective mass comprise at least one of electrons and holes.

60. A method according to Claim 57 wherein each base semiconductor portion comprises silicon.

61. A method according to Claim 57 wherein each energy band-modifying layer comprises oxygen.

62. A method according to Claim 57 wherein each energy band-modifying layer is a single monolayer thick.

63. A method according to Claim 57 wherein each base semiconductor portion is less than eight monolayers thick.

64. A method according to Claim 57 wherein each base semiconductor portion is two to six monolayers thick.

65. A method according to Claim 57 wherein the superlattice further has a substantially direct energy bandgap.

66. A method according to Claim 57 wherein the superlattice further comprises a base semiconductor cap layer on an uppermost group of layers.

67. A method according to Claim 57 wherein all of the base semiconductor portions are a same number of monolayers thick.

68. A method according to Claim 57 wherein at least some of the base semiconductor portions are a different number of monolayers thick.

69. A method according to Claim 57 wherein all of the base semiconductor portions are a different number of monolayers thick.

70. A method according to Claim 57 wherein each non-semiconductor monolayer is thermally stable through deposition of a next layer.

71. A method according to Claim 57 wherein each base semiconductor portion comprises a base semiconductor selected from the group consisting of Group IV semiconductors, Group III-V semiconductors, and Group II-VI semiconductors.

72. A method according to Claim 57 wherein each energy band-modifying layer comprises a non-semiconductor selected from the group consisting of oxygen, nitrogen, fluorine, and carbon-oxygen.

73. A method according to Claim 57 wherein forming the superlattice comprises forming the superlattice on a substrate.

74. A method according to Claim 57 wherein the lower conductivity effective mass is less than two-thirds the conductivity effective mass that would otherwise occur.

75. A method according to Claim 57 further comprising doping the superlattice with at least one type of conductivity dopant therein.

76. A method according to Claim 57 wherein the superlattice defines a channel for the semiconductor device and wherein forming the regions comprises:

forming source and drain regions laterally adjacent the superlattice channel; and

forming a gate overlying the superlattice channel.